library ieee;

use ieee.std\_logic\_1164.all;

entity D\_FF is

port(d,reset: in std\_logic;

q,nq: out std\_logic);

end D\_FF;

architecture D of D\_FF is

signal clk: std\_logic:= '0';

begin

tact: process(clk)

begin

clk <= not clk after 50 ns;

end process tact;

process(clk, reset)

begin

if reset='1' then

q<= '0';

nq<= '1';

elsif clk='1' and clk'event then

q<=d;

nq<= not d;

end if;

end process;

end D;